CLAIMS:

What is claimed is:

Sub B1

1. A method of managing a network switch having a processor card including a memory and a processing unit in the processor card comprising:

detecting an error;

determining a type of the error;

determining whether a threshold has been reached; and,

performing a hitless rebuild in the processor card when the type of the error is in a first set of errors and the threshold has not been reached.

2. The method of claim 1, wherein the step of performing the hitless rebuild includes:

performing an initialization of the memory; and,

protecting a portion of the memory from access by the processing unit during the initialization.

3. The method of claim 1, wherein performing a hitless rebuild includes protecting a portion of the memory that contains a set of routing tables.

4. The method of claim 1, wherein performing a hitless rebuild includes protecting a portion of the memory that contains a set of state tables.

5. The method of claim 1, wherein the memory is accessed through a set of memory addresses and performing a hitless rebuild includes preventing the processing unit from accessing a predetermined set of memory addresses in the set of memory addresses.

6. The method of claim 1, wherein determining the type of the error includes identifying a non-ignorable error.

7. The method of claim 1, further including setting the processing unit to enter into a degraded mode when the type of the error is in the first set of errors and the threshold has been reached.

8. The method of claim 1, wherein determining whether the threshold has been reached includes:

determining a number of hitless rebuilds that has been performed in the processor card;

determining a time period from a first hitless rebuild time and a second hitless rebuild time; and,

determining whether the number of hitless rebuilds versus the time period has reached a ratio.

Sub B3

9. An apparatus for managing a network switch having a processor card including a memory and a processing unit in the processor card comprising:

means for detecting an error;

means for determining a type of the error;

means for determining whether a threshold has been reached; and,

means for performing a hitless rebuild in the processor card when the type of the error is in a first set of errors and the threshold has not been reached.

10. An article comprising a computer readable medium having instructions stored thereon, which when executed, causes:

detection of an error;

determination of a type of the error;

determination of whether a threshold has been reached; and,

performance of a hitless rebuild in a processor card when the type of the error is in a first set of errors and the threshold has not been reached.

11. The article of claim 10, wherein the computer readable medium further having instructions stored thereon, which when executed, causes:

performance of an initialization of the memory; and,

protection of a portion of the memory from access by the processing unit during the initialization.

12. The article of claim 10, wherein the computer readable medium further having instructions stored thereon, which when executed, causes:

performance of a hitless rebuild includes the step of protecting a portion of the memory that contains a set of routing tables.

13. The article of claim 10, wherein the computer readable medium further having instructions stored thereon, which when executed, causes:

protecting a portion of the memory that contains a set of state tables.

14. The article of claim 10, wherein the memory is accessed through a set of memory addresses and the computer readable medium further having instructions stored thereon, which when executed, causes:

prevention of a processing unit from accessing a predetermined set of memory addresses in the set of memory addresses.

15. The article of claim 10, wherein the computer readable medium further having instructions stored thereon, which when executed, causes:

identification of a non-ignorable error.

16. The article of claim 10, wherein the computer readable medium further having instructions stored thereon, which when executed, causes:

setting of the processing unit to enter into a degraded mode when the type of the error is in the first set of errors and the threshold has been reached.:

17. The article of claim 10, wherein the computer readable medium further having instructions stored thereon, which when executed, causes:

determination of a number of hitless rebuilds that has been performed in the processor card;

determination of a time period from a first hitless rebuild time and a second hitless rebuild time; and,

determination whether the number of hitless rebuilds versus the time period has reached a ratio.

add B5

add C'

add D'